SYNOPSYS®

Multiphysics Fusion Technology for Multi-Die Designs Explained

Table of Contents

3 Multiphysics is No Longer a Downstream Problem

4 What is Multiphysics Simulation, and Why is it Needed?

6 What are Multiphysics Effects?

7 Thermal Effects

8 Power Integrity Effects

9 Electromagnetic Effects

10 Multiphysics Solutions

11 Multiphysics Solutions for Continuous Validation

12 Multiphysics Fusion Technology for Multi-Die Designs

13 Thermal Analysis Signoff

15 Power Integrity Signoff

17 Signal Integrity Signoff

19 Static-Timing Signoff

21 Gold-Standard Multiphysics Analysis and Signoff with Synopsys

22 About Synopsys

Multiphysics Is No Longer a Downstream Problem

What's driving this shift?

- **Advanced Packaging Adoption**
  Multi-die designs integrate multiple dies (also called chiplets) stacked or placed side-by-side in a single package, increasing interactions among thermal, electrical, and mechanical domains. Multiphysics analysis is needed to solve these interactions together and avoid late-stage surprises.
- **Miniaturization and Density**
  Shrinking geometries and higher component density magnify challenges such as heat dissipation, power delivery, and signal integrity (SI). Multiphysics analysis is essential to ensure reliability and performance at these scales.
- **Heterogeneous Integration**
  Combining different types of dies using different process technologies in a single package means diverse materials and operating conditions. Multiphysics analysis helps you address cross-domain effects like thermal stress impacting reliability and electrical performance.
- **Reliability and Yield Pressure**
  As multi-die designs become more complex, risks of failure due to thermal hotspots, electromigration (EM), electrostatic discharge, and mechanical stress increase. Multiphysics modeling enables early identification and mitigation of these risks, supporting higher yield and reliability.
- **Faster Time-to-Market**
  Competitive pressure drives rapid development cycles. Multiphysics simulation tools allow you to accelerate design iterations by predicting cross-domain issues earlier and reduce physical prototyping with virtual analysis.
- **Regulatory and Customer Demands**
  Automotive, AI, data centers, and consumer electronics markets require robust, reliable performance. Comprehensive multiphysics analysis is necessary to meet stringent safety and reliability standards.

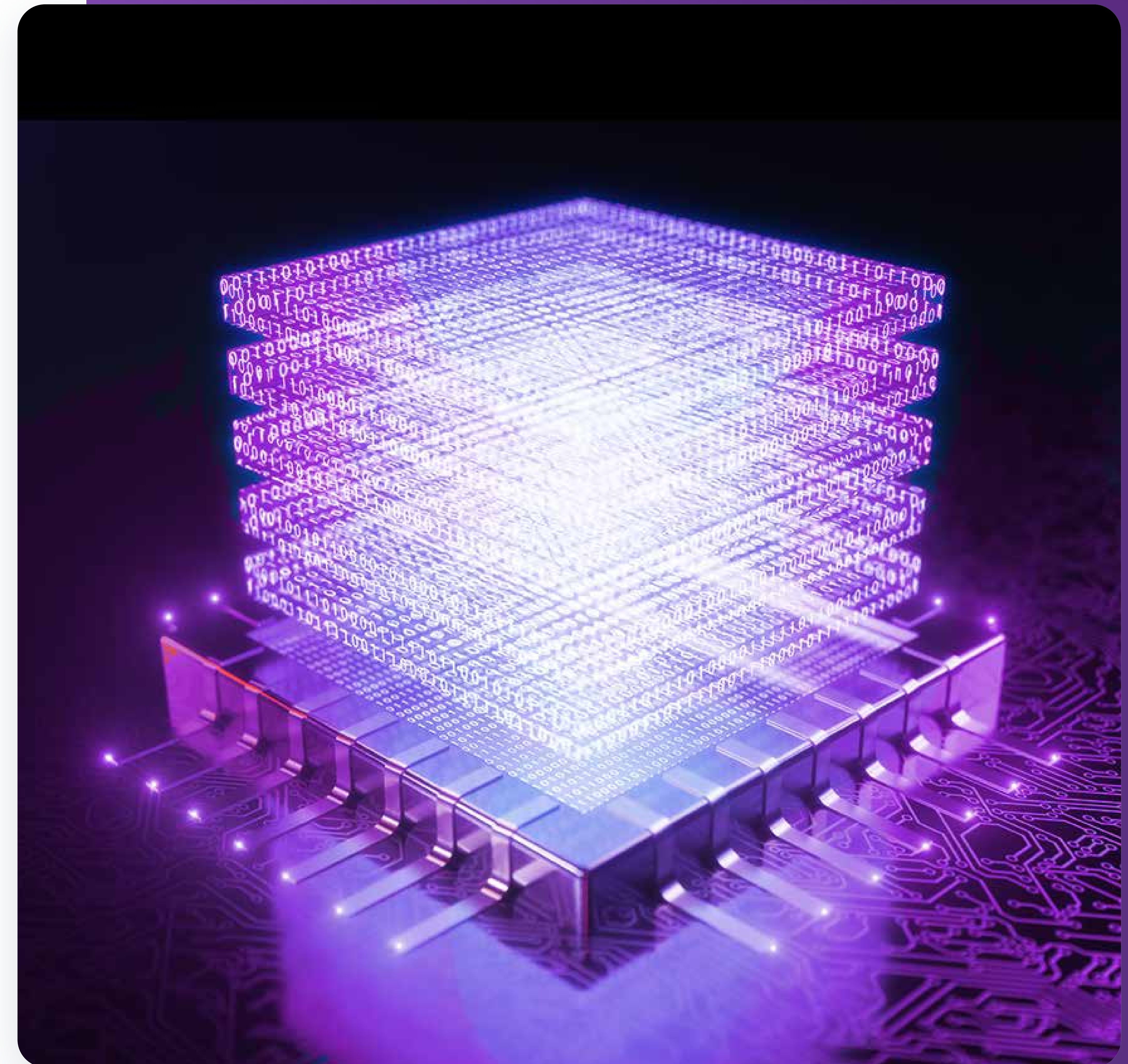
What is Multiphysics Simulation, and Why is it Needed?

Multiphysics simulation is the integrated modeling and analysis of multiple physical and electrical phenomena that affect the performance, reliability, and manufacturability of semiconductor devices.

Multi-die designs mark a fundamental shift in semiconductor engineering. These large, complex designs have introduced a range of unfamiliar multiphysics effects.

Some of the key multiphysics issues include electrical, thermal, electromagnetic, and electromechanical effects.

> With today's multi-die designs, multiphysics effects have worsened as integration complexity and inter-die communication challenges intensify.



> "Multi-die packaging fundamentally changes how chips are designed. Engineers must incorporate electrical, thermal, and electromagnetic analysis into the core electronics design flow to identify and resolve issues early, before they become costly or irreversible."

- Sassine Ghazi, Synopsys CEO

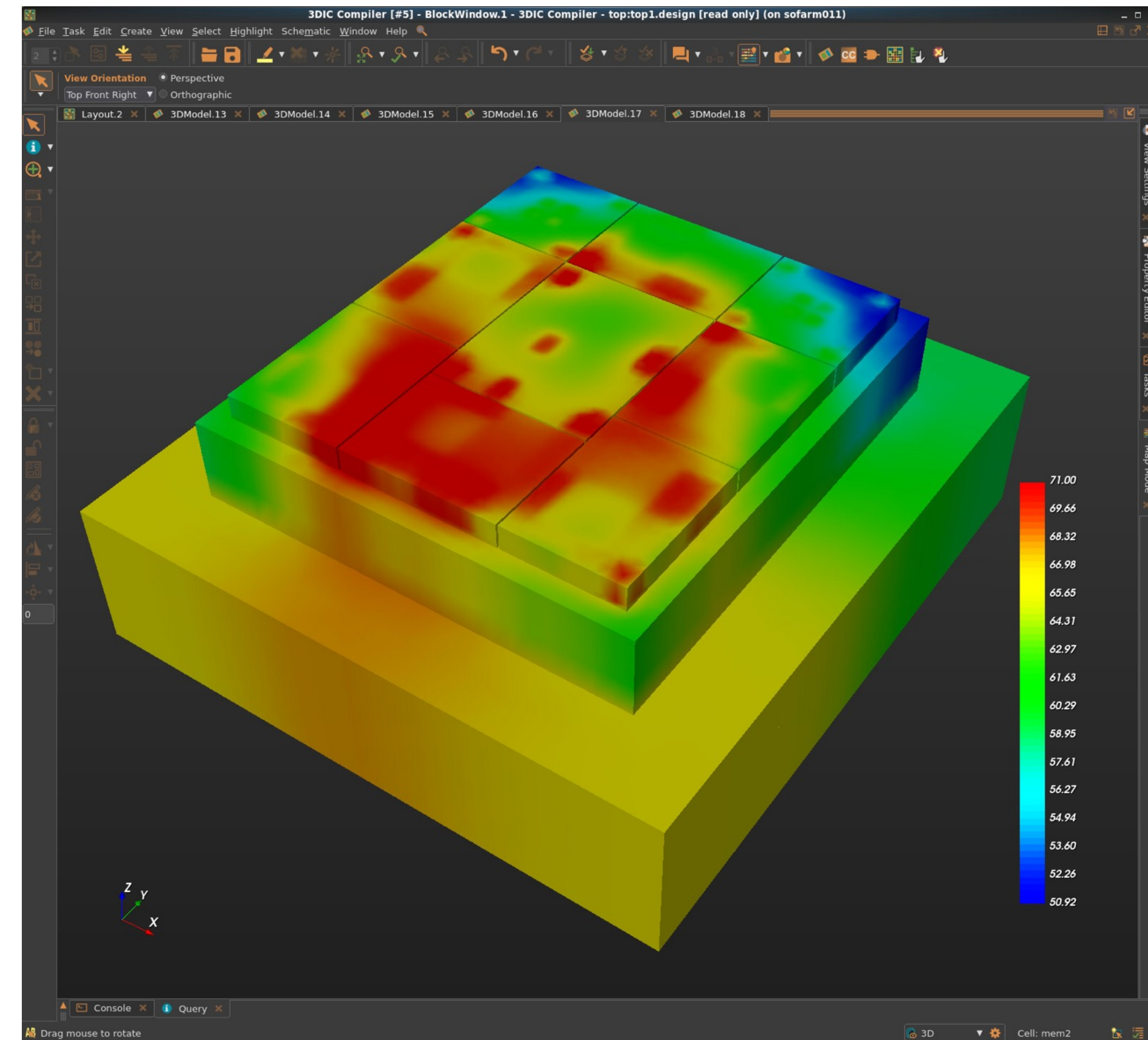
What are Multiphysics Effects?

- Thermal Effects
- Power Integrity Effects
- Electromagnetic Effects
- Other Effects

Thermal Effects

- **Heat Dissipation**
  Multiple high-performance dies generate significant heat, which can lead to hotspots and uneven temperature distribution.
- **Thermal Coupling**
  Heat from one die can affect neighboring dies, impacting performance and reliability.
- **Cooling**
  Stacked or closely packed dies complicate heat removal and may require advanced thermal management solutions.

3D Model of Thermal Heat Map in 3DIC Compiler



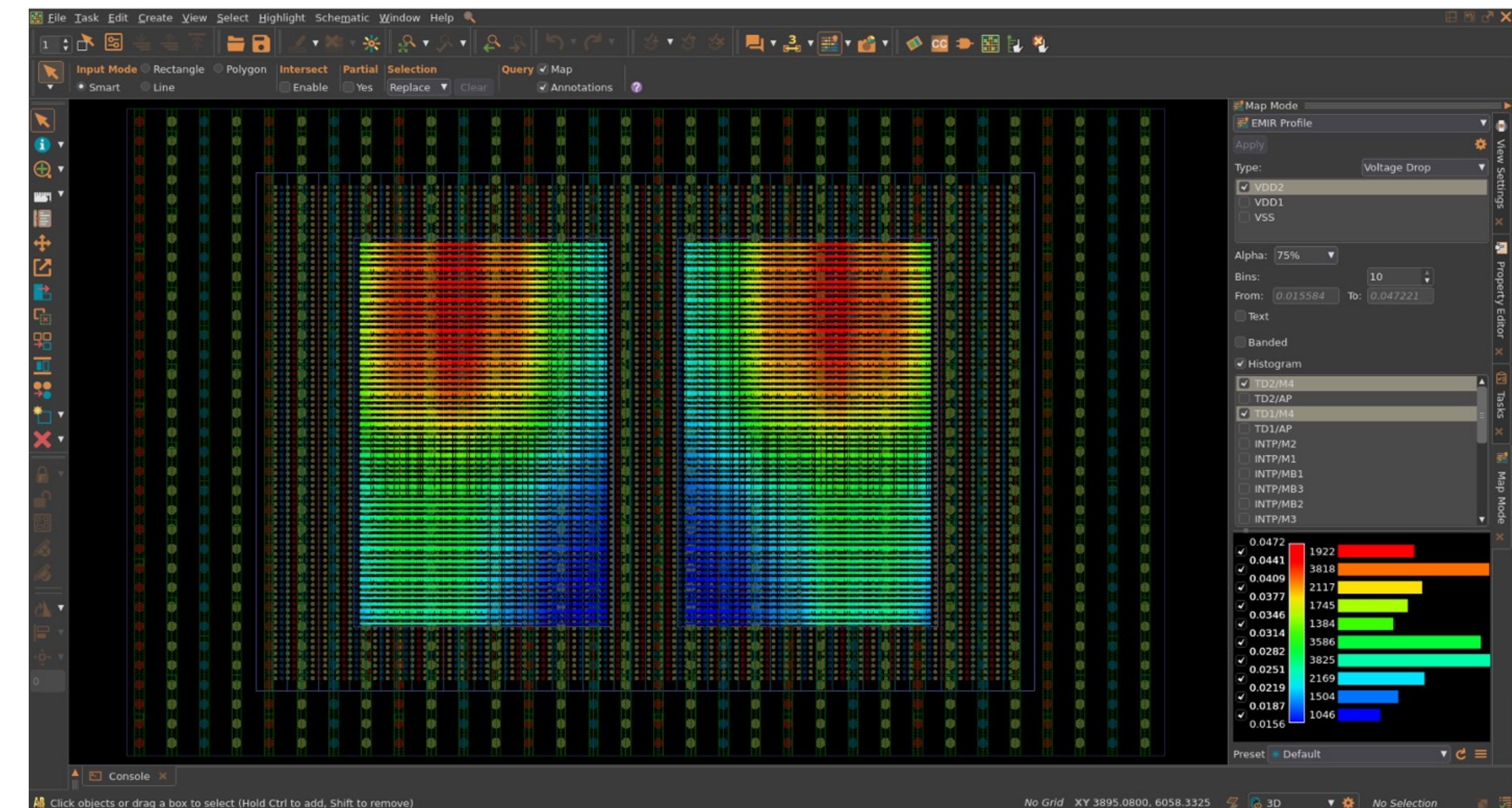
Power Integrity Effects

- **Complex Power Distribution Networks**
  They can conduct hundreds of watts of power across packaging leads, through-silicon vias (TSVs), and thousands of micro-bump connectors. This complexity is compounded by the trend to include integrated voltage regulators (IVRs) with the power network inside the connectivity substrate.

- **Razor-thin Voltage Margins**
  In today's ultra-low voltage process technologies, voltage drop (also known as IR drop) reduces circuit performance and can lead to functional failure and timing challenges.

- **Electromigration**
  Electromigration can compromise the integrity of a design if interconnects carry too much current. Electromigration is a slow effect that degrades wires over weeks or years leading to catastrophic product failure.

IR Drop Analysis Heat Map in 3DIC Compiler

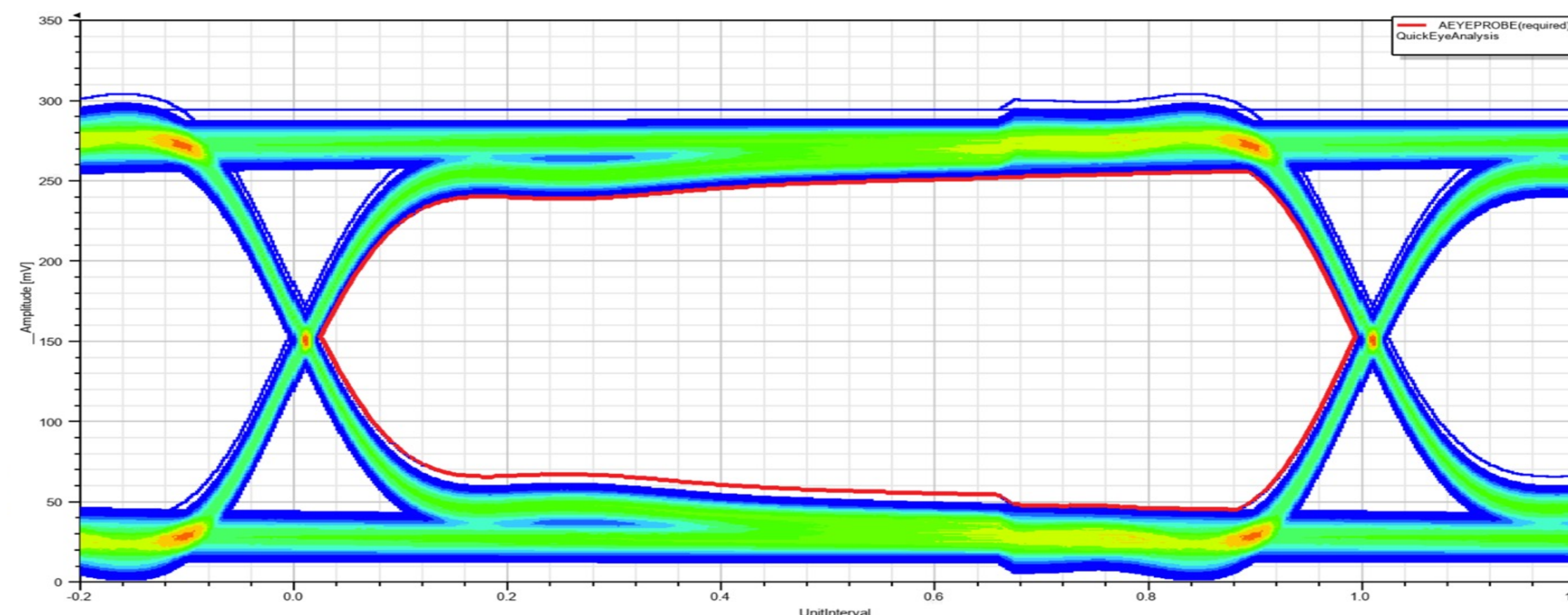


Electromagnetic Effects

- **Transmission Lines**
  Long, high-speed signal routing on large package substrates and interposers behave like transmission lines which introduce electromagnetic effects due to insertion loss, coupling, ringing, and impedance mismatch.

- **Signal Integrity**
  Crosstalk, electromagnetic interference, and parasitic capacitance/inductance are more pronounced in densely packed multi-die designs.

Eye Diagram Showing Optimized Signal Integrity



Other Effects

- **Thermomechanical Stress**
  Differences in material properties and thermal expansion cause mechanical stress and warping, potentially leading to cracking or delamination.

- **Layout Dependent Effects (LDE)**
  Multiphysics interactions amplify the impact of process variations at advanced processes, leading to complex variations in electrical parameters.

Multiphysics Solutions

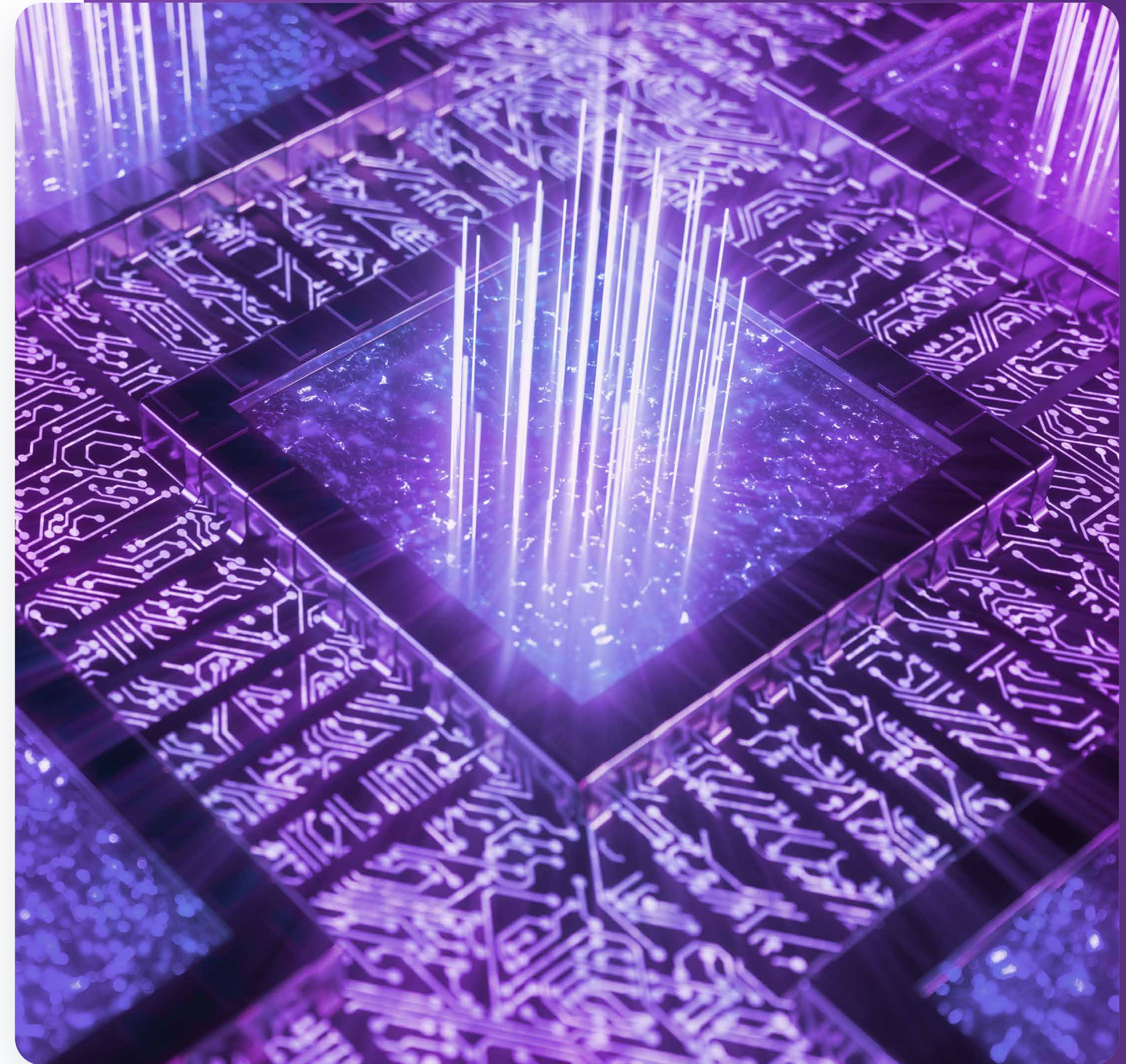
- Thermal Analysis Signoff
- Power Integrity Signoff
- Signal Integrity Signoff
- Static-Timing Signoff

Multiphysics Solutions for Continuous Validation

2.5D and 3D multi-die designs mark a fundamental shift in traditional semiconductor design. These technologies have introduced chip designers to a range of multiphysics effects not experienced in monolithic chips.

These challenges create an unprecedented need for multiphysics simulation and analysis throughout the entire multi-die design journey, not only after the full design is complete, when it's too late or too costly to address multiphysics-related issues.

> **Synopsys provides a foundry-certified multiphysics simulation and analysis solution within 3DIC Compiler, a unified exploration-to-signoff platform for multi-die designs.**



Multiphysics Fusion Technology for Multi-Die Designs

Synopsys' Multiphysics Fusion™ Technology, the first in a broader roadmap of EDA solutions, brings together Synopsys' industry-leading silicon design tools with the gold-standard signoff analysis capabilities from Ansys.

These differentiated technologies help engineering teams achieve better power, performance, and area (PPA) and faster time-to-results. Synopsys Multiphysics Fusion Technology for Multi-Die Design offers thermal analysis and power integrity optimization across the full EDA stack, from early floorplanning to signoff, in addition to high-speed auto-routing with AI-driven signal integrity optimization that enables early thermal, IR, and stress analysis.

The multiphysics solution, available within Synopsys' 3DIC Compiler platform for multi-die/advanced package co-design and optimization, helps designers predict thermal effects, mechanical stress, and electromagnetic effects.

Early prototyping capabilities verify feasibility and optimize architectural choices based on real long-duration activity profiles from RTL simulation. The time constant for thermal effects is much longer than that for electrical phenomena, so thermal activity must be simulated over seconds or longer. The Synopsys ZeBu® Emulation System provides an efficient source of realistic thermal activity patterns.

Efficient reduced order models (ROMs) deliver fast and accurate hierarchical analysis of a full multi-die design through data reduction and efficient scaling in the cloud.

> **By providing highly accurate simulations, Synopsys enables faster design cycles and improved reliability, helping you address complex multiphysics challenges with confidence.**

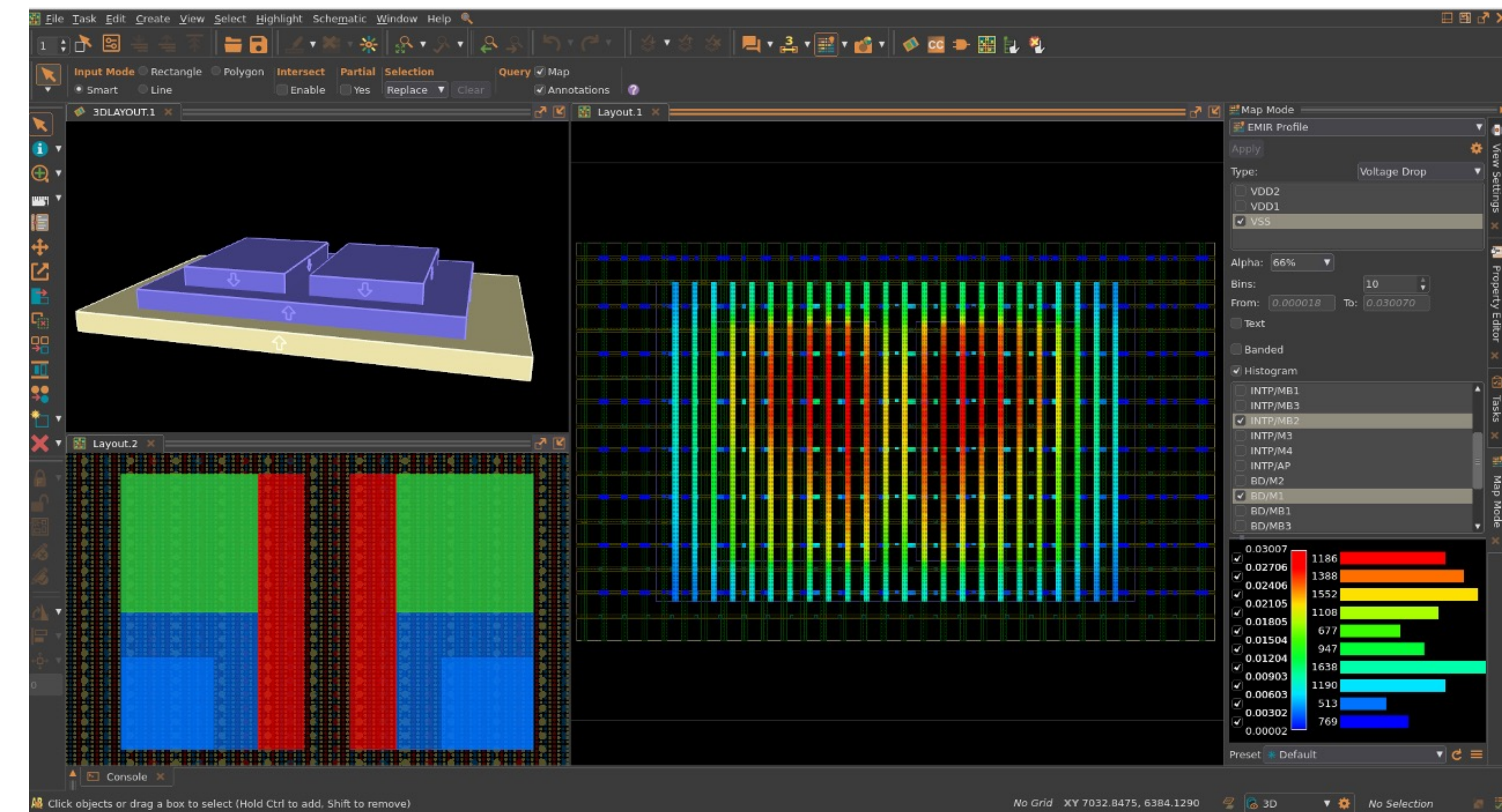
Thermal Analysis Signoff

Overheating and thermo-mechanical stresses impact almost every aspect of system design and reliability. Maximum system temperature depends on board-level cooling as well as the chip-level sources of heat from transistor switching. This creates a complex challenge for creating efficient thermal models and simulating accurately across six orders of magnitude—from nanometers to centimeters.

EDA tools should be able to analyze a complete multi-die design in a board-level context.

Thermal management is the #1 issue facing multi-die designers.

Thermal Heat Map with TSVs in 3DIC Compiler



Redhawk-SC Electrothermal™ analyzes entire multi-die designs with power sources supplied by RedHawk-SC™ voltage-drop analysis and system boundary conditions from Ansys Icepak® electronics cooling simulation software. RedHawk-SC Electrothermal will also calculate the mechanical stresses and warpage due to thermal gradients.

RedHawk-SC Electrothermal combines the chiplet models, the interposer model, and the package model for comprehensive co-simulation of the entire power distribution network (PDN) in one place. In addition to the electrical models, RedHawk-SC Electrothermal also generates both low-frequency and high-frequency power noise as an input to the SPICE transient simulation of the PDN. The results show voltage transients in the time domain as well as resonant frequencies for the PDN in the frequency domain.

> **Accurate thermal prototyping, analysis, and signoff including local and system heating is critical.**

> **Synopsys' RedHawk-SC Electrothermal™ is a proven thermal and multiphysics simulation solution. A purpose-built analysis tool for thermal and mechanical simulations of 2.5D/3DIC multi-die designs.**

Synopsys' thermal and mechanical simulation engines have decades of proven experience, while RedHawk-SC is the market leader in voltage drop analysis. Together they form the most accurate and comprehensive solution on the market.

Building on RedHawk-SC Electrothermal's ability to analyze entire multi-die designs with system boundary conditions and power sources, the Synopsys Chip Thermal Model (CTM) enables very high system capacity with reduced-order hierarchical modeling.

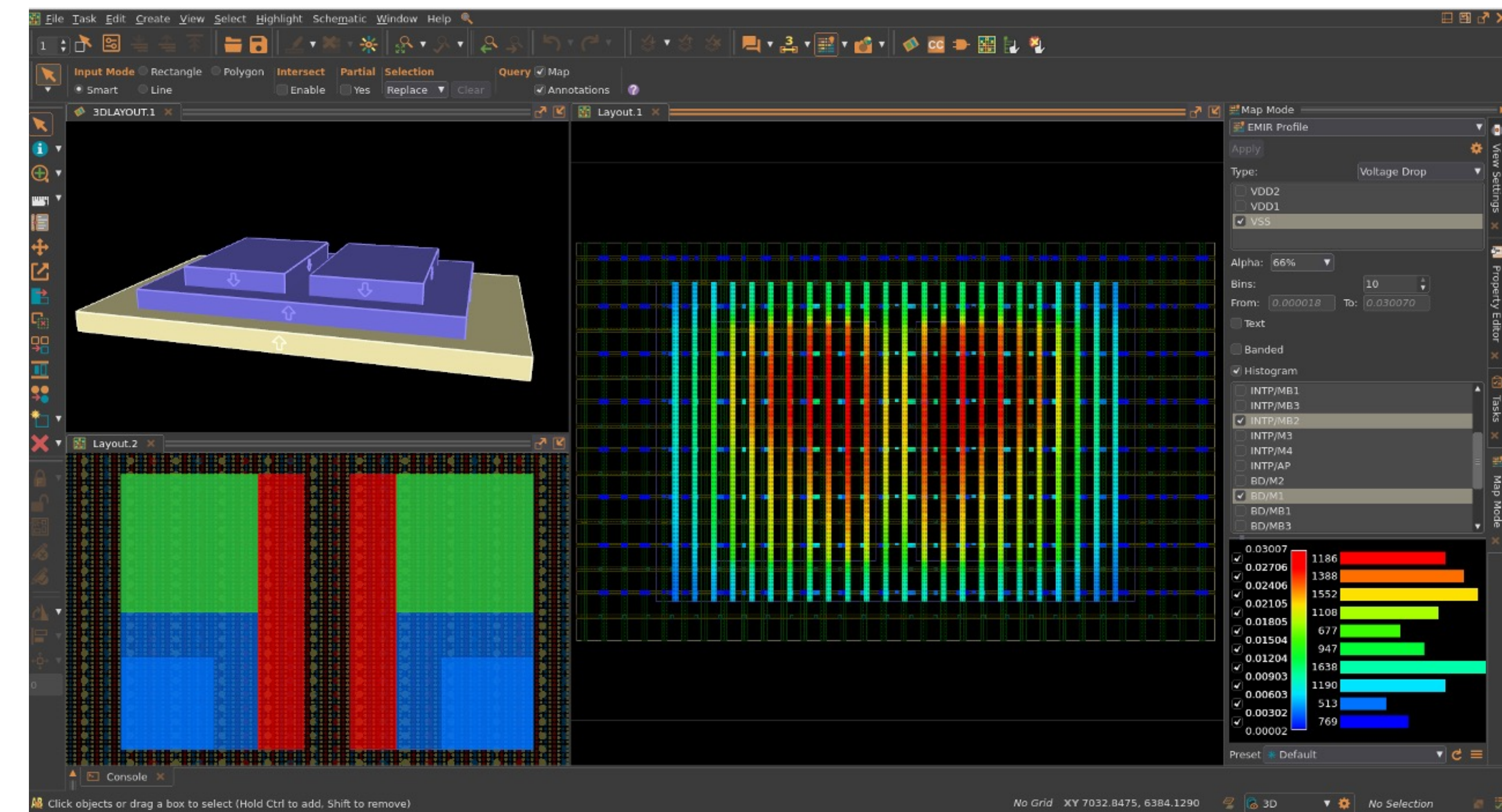
Power Integrity Signoff

The challenge to reliably distribute hundreds of watts of power. Multi-die designs can contain a dozen dies or more, an interposer, deep-trench decoupling capacitors, and a substrate package. This results in extremely large power networks that must distribute significant power through many thousands of three-dimensional connections.

This creates a classic multi-scale problem where nano-scale transistor switching causes voltage drops that must be modeled at the centimeter level. Also, vertical connections like TSVs and hybrid bumps must be modeled in detail for accurate results.

> **Accurate hierarchical techniques are required to enable fast full-system voltage drop verification, and the ability to analyze high-frequency chip noise together with low-frequency system noise.**

Multi-View IR Drop Heat Map in 3DIC Compiler

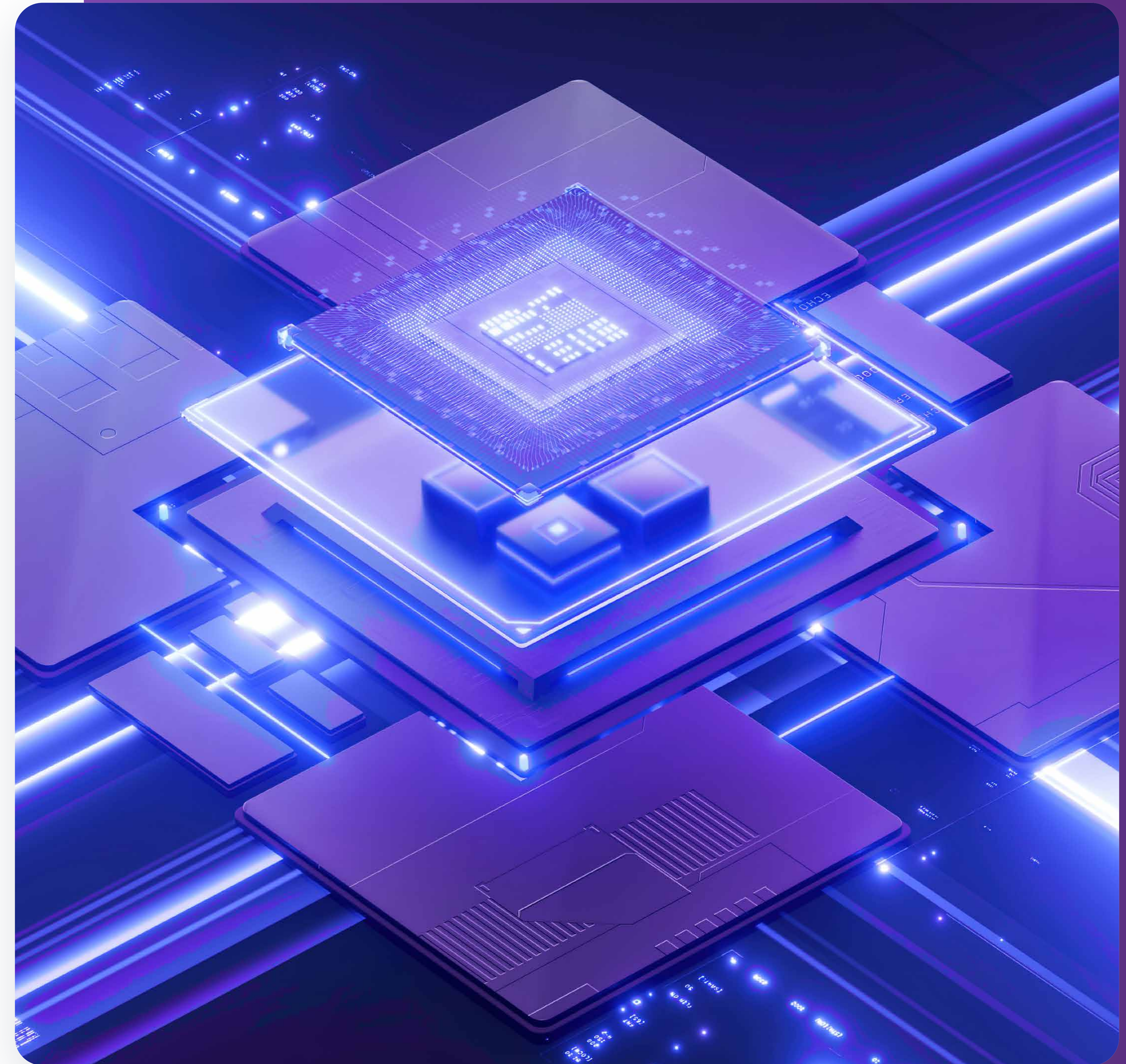


RedHawk-SC's high-capacity, distributed voltage-drop analysis uses Synopsys' Chip Power Model (CPM) for fast turn-around of full multi-die design analysis. RedHawk-SC creates, assembles, and manages these models to simulate the entire design to calculate voltage drop and electromigration in every part of the multi-die stack, with minimal accuracy loss.

RedHawk-SC is unique in its ability to harness all the simulation capabilities across analog, digital, electrostatics, and activity profiling to deliver accurate and reliable results that remove the need for expensive and wasteful safety margins that reduce system performance.

Synopsys Totem-SC™, a transistor-level power integrity and reliability analysis solution, will generate CPMs for entire HBM memories and other analog components. And Synopsys PathFinder-SC™ is foundry-certified to signoff electrostatic discharge safety across multiple chips.

> **Synopsys RedHawk-SC™ has sophisticated hierarchical power modeling for full-system reliability.**



Signal Integrity Signoff

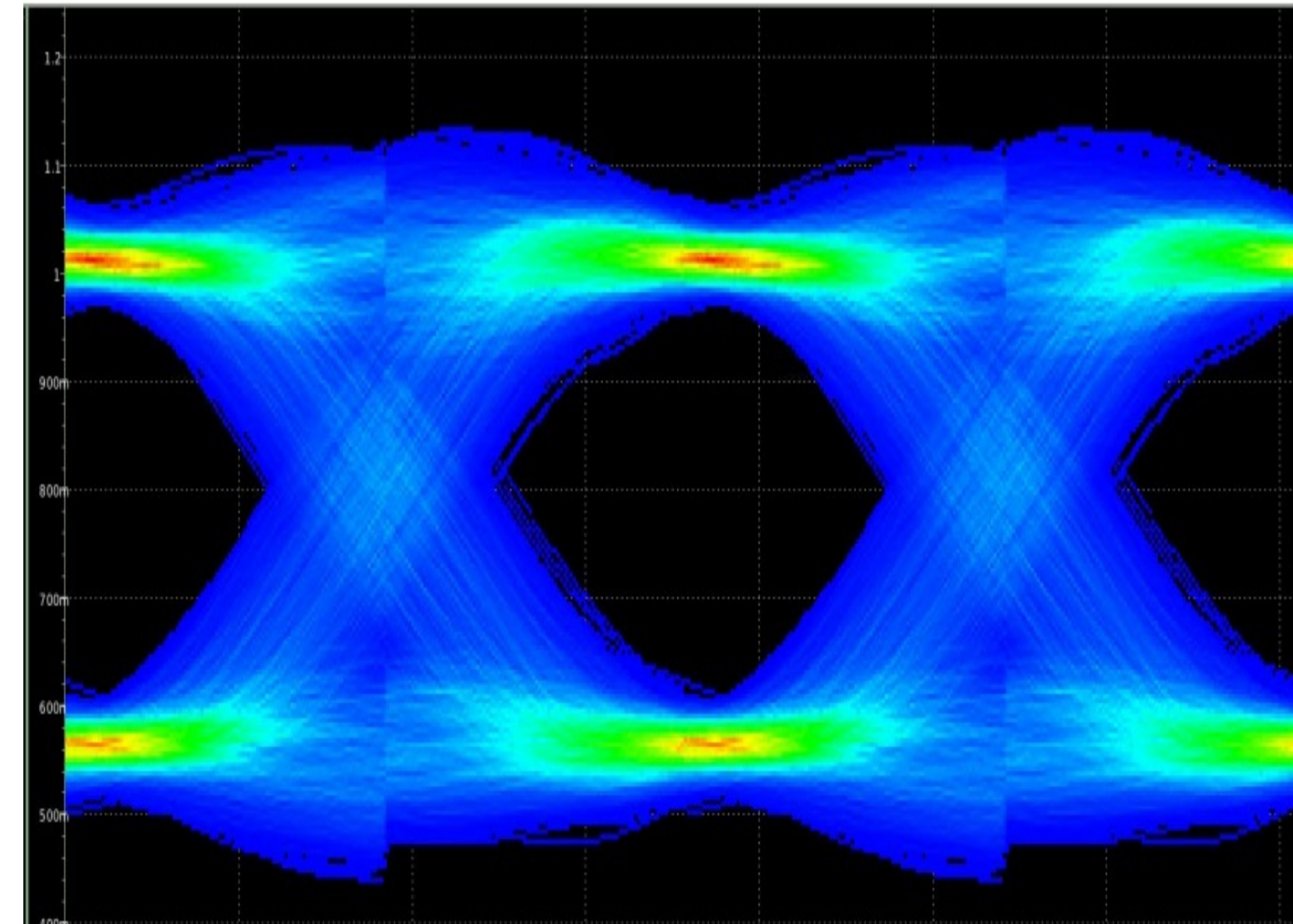
High-speed interposer signals become analog. Digital interconnect channels between dies, using SerDes, PHY, UCIe, or HBM protocols, experience significant electromagnetic coupling and interference that requires them to be extracted with electromagnetically coupled models.

While common in radio-frequency design, electromagnetic extraction is new to most digital designers, and they often lack the expertise and tools for this. Also, the size of interposers is a significant challenge to most existing extractors designed for typically small analog designs.

These trends are blurring the lines between chips and systems, which is changing the way design teams are composed, combining package experts with chip layout experts.

> **Efficient, accurate electromagnetic models for the full signal path across an interposer, package, and board are critically important.**

Eye Diagram of a High-Speed Signal

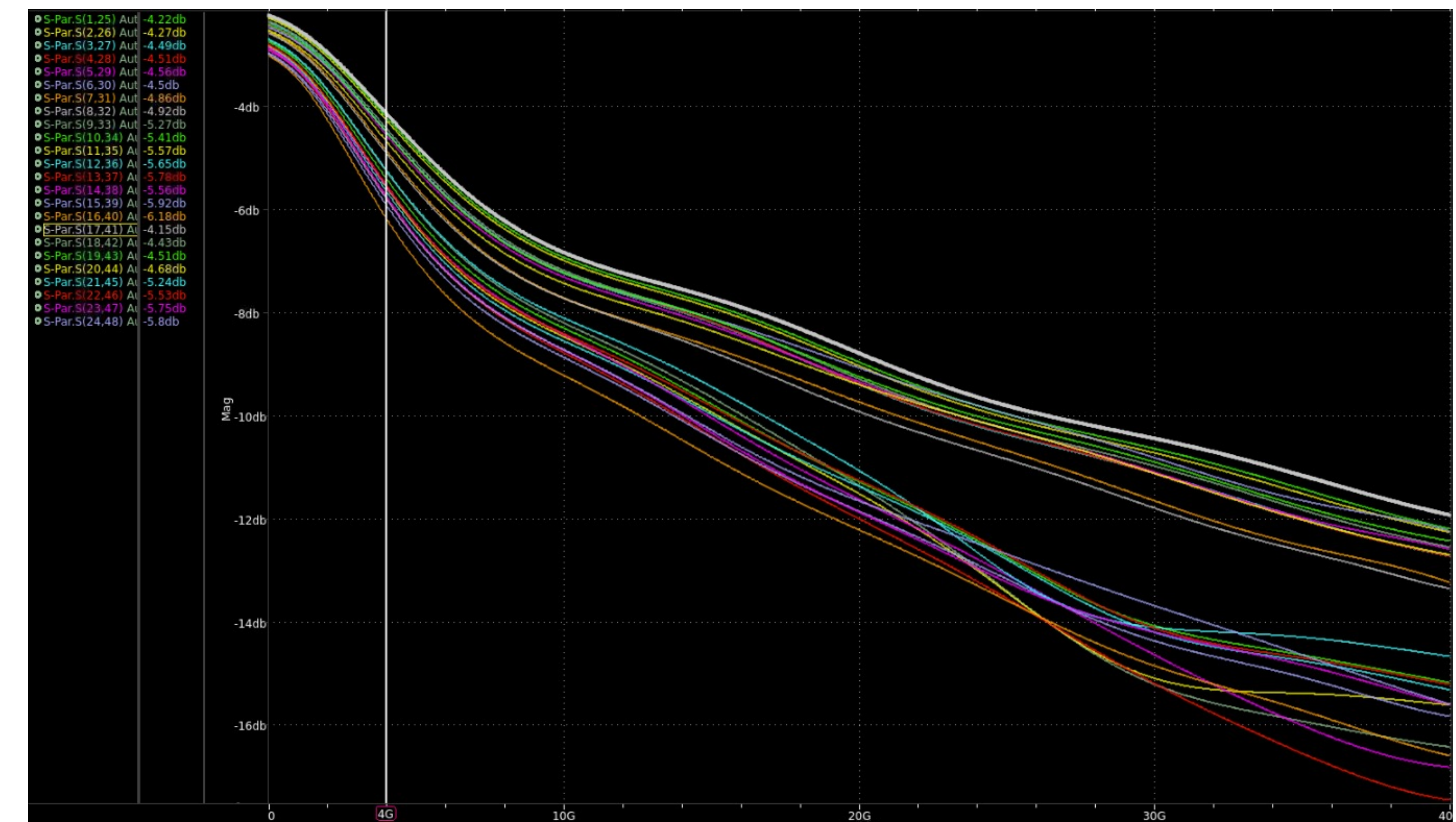


Synopsys HFSS-IC™ delivers the speed, capacity, and accuracy to extract resistance inductance capacitance and reluctance (RLCk) loss or S-parameter models of entire communication channels on a multi-die design, including the extraction of through-silicon vias (TSVs) needed for on-silicon and system-level electromagnetics (EM).

Hierarchical models enable large-scale multi-die signal integrity analysis. Its high capacity means accuracy is maintained by avoiding the need to divide a design into smaller pieces.

As a result, HFSS-IC is easier to use and delivers more accurate results for high-speed interconnect modeling. This saves time and reduces the need for safety margins.

Insertion Loss Plots in 3DIC Compiler



HFSS-IC's relied-on accuracy is foundry-certified for signoff electromagnetic extraction by all leading foundries.

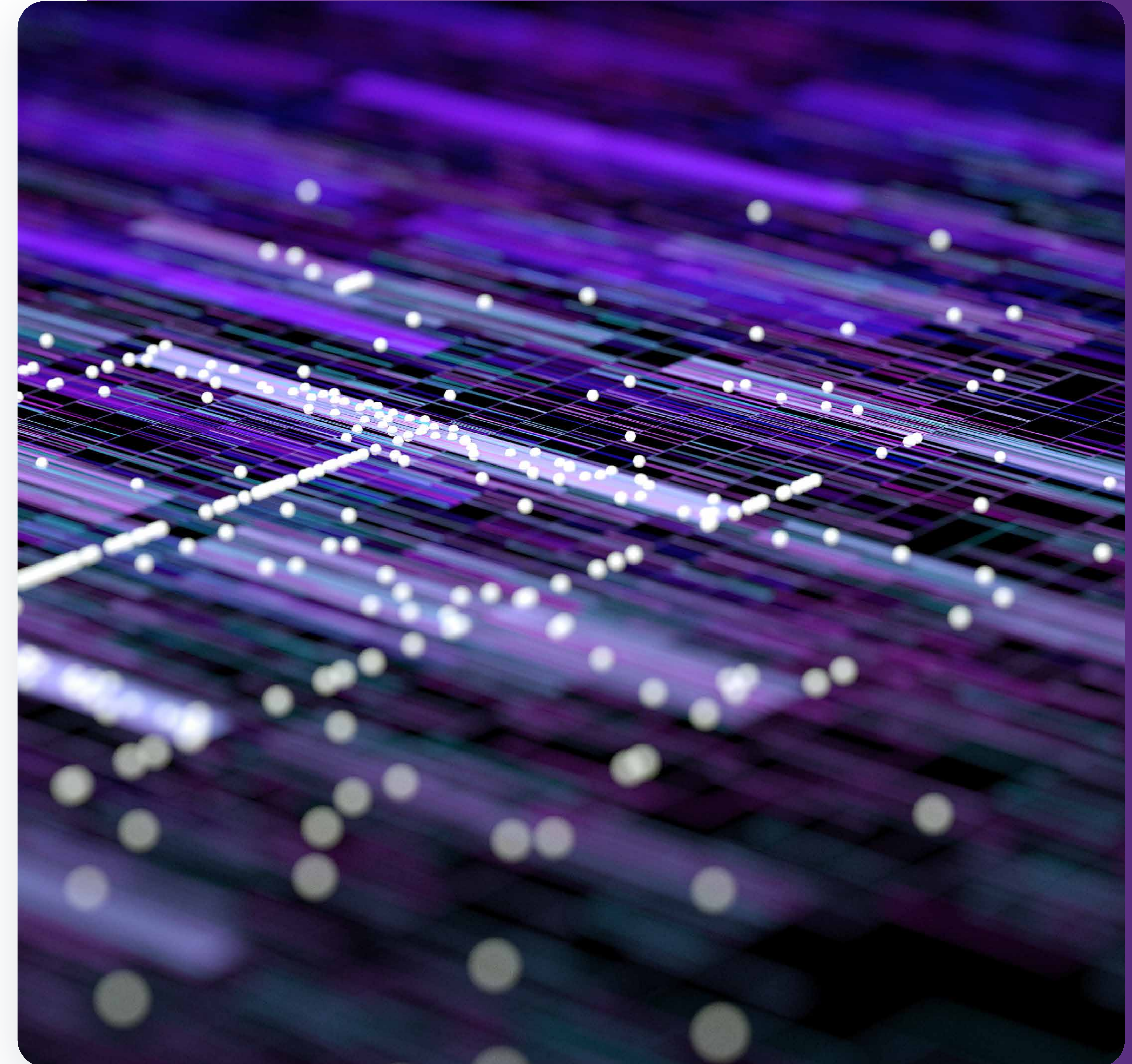
Synopsys HFSS-IC™ delivers fast, high-capacity electromagnetic modeling for interposer SI.

Static-Timing Signoff

Static-timing analysis (STA) has become more challenging and complex. Margin-based timing analysis is no longer sufficient. Multi-die designs can employ multiple process technologies from multiple silicon vendors. STA needs to be able to perform analysis using multiple timing libraries with different process, temperature, and voltage parameters as well as delay data.

Parasitic networks must be constructed involving multiple dies, interposers, and organic substrates. The number of timing corners and scenarios multiplies and must be managed and optimized. Noise and IR-drop from numerous elaborate power networks must be accounted for, as well as being SI-, thermal-, and stress-aware.

> **Synopsys PrimeTime™ delivers next generation integrated, multiphysics-aware signoff STA.**



PrimeTime’s transition from margin-based to native multiphysics timing signoff combined with Synopsys’ multiphysics simulation and analysis solutions reduces pessimism and increases timing analysis accuracy.

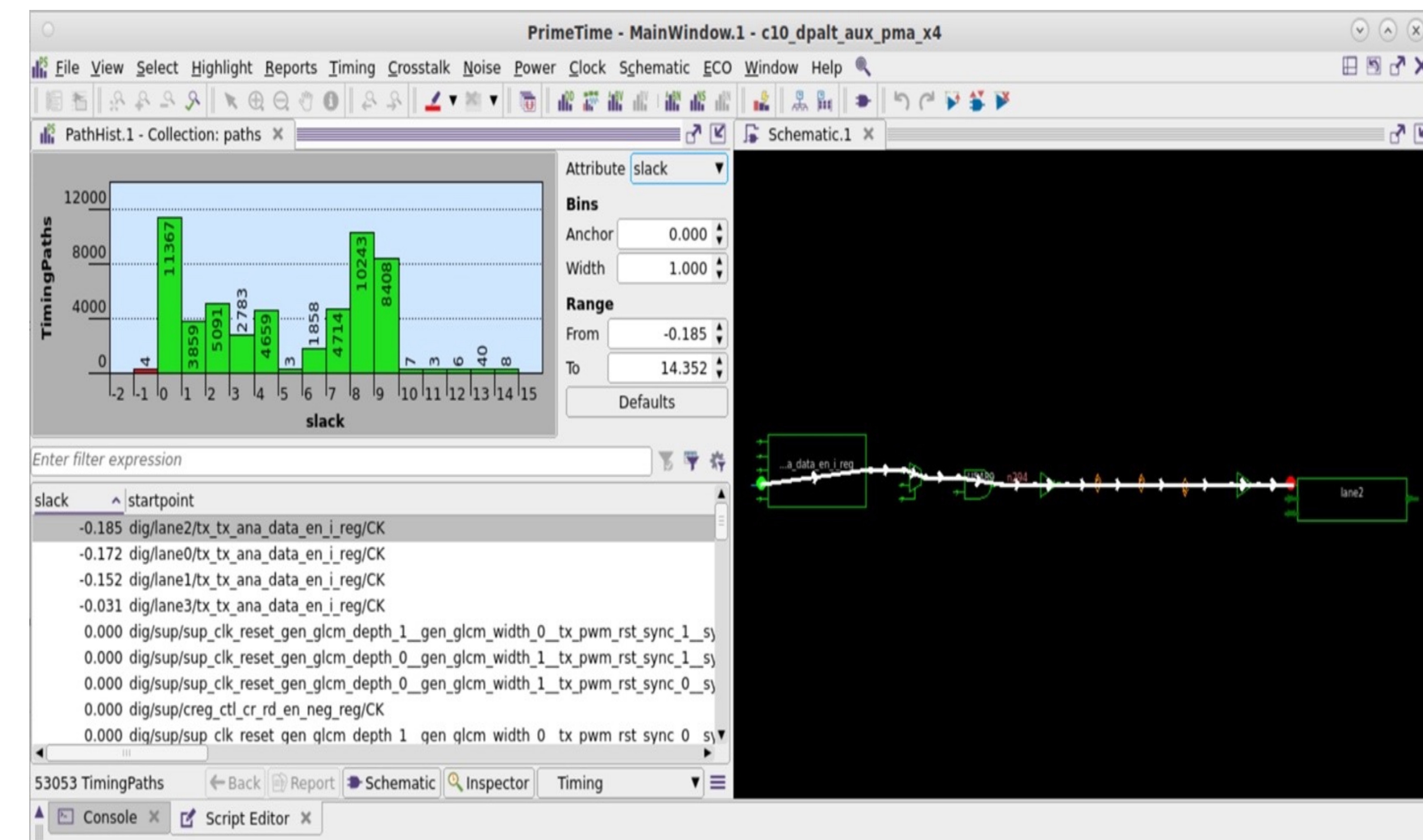
Next-generation, IR-aware STA achieves SPICE-accurate, IR-aware timing across all scenarios for robust signoff.

Thermal-aware STA analyzes the thermal effects on timing for reliable performance, and stress-aware STA accounts for thermal-induced mechanical stress for accurate timing closure.

PrimeTime provides coverage for all STA scenarios across the entire multi-die design, optimizing timing from simulated voltage, thermal, and stress conditions.

> **PrimeTime is proven and foundry-certified over multiple decades as the industry-standard STA solution.**

Timing Slack Histogram and Logic Path in PrimeTime

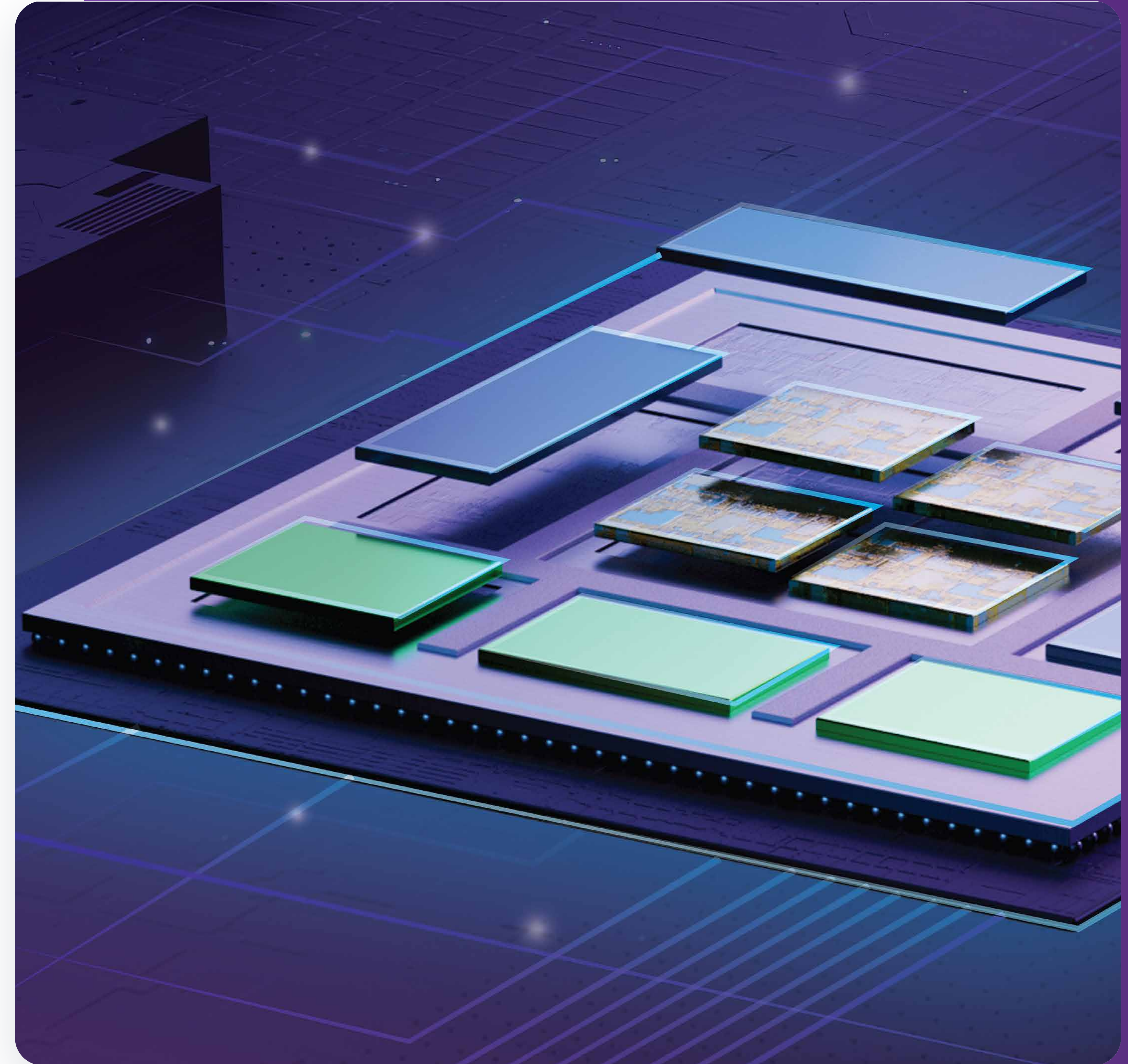


Gold-Standard Multiphysics Analysis and Signoff with Synopsys

Synopsys delivers a uniquely integrated approach to multiphysics analysis, enabling you to address the complex interactions among electrical, thermal, and electromagnetic domains within multi-die design.

Through Multiphysics Fusion™ Technology, Synopsys brings together industry-leading silicon design tools with the gold-standard signoff analysis capabilities. The 3DIC Compiler platform seamlessly incorporates RedHawk-SC for power integrity analysis, RedHawk-SC Electrothermal for dynamic thermal analysis, and HFSS-IC for high-frequency electromagnetic modeling, within a unified environment. This integration enables concurrent EMIR, thermal, signal integrity, and electromechanical stress signoff, ensuring accuracy and reliability throughout the design stack.

You can rapidly iterate through partitioning, floorplanning, routing, and verification, guided by multiphysics feedback.



About Synopsys

We live in a world where intelligent technology is everywhere, shaping our daily lives. This pervasive intelligence is driven by three major trends: artificial intelligence, software-defined systems and silicon proliferation. For decades we've been a driving force of the technologies that make pervasive intelligence possible.

Synopsys is the leader in engineering solutions from silicon to systems, enabling customers to rapidly innovate AI-powered products. We deliver industry-leading silicon design, IP and simulation and analysis solutions. We partner closely with our customers across a wide range of industries to maximize their R&D capability and productivity, powering innovation today that ignites the ingenuity of tomorrow. Companies trust Synopsys to pioneer new technologies to help them get to market faster, without compromise.

Our Technology, Your Innovation™

© 2026 Synopsys, Inc. and/or Ansys, Inc. All Rights Reserved. Synopsys is a trademark of Synopsys, Inc. in the United States and other countries. A list of Synopsys trademarks is available at http://www.synopsys.com/copyright.html. All other names mentioned herein are trademarks or registered trademarks of their respective owners. snps4431367651